COMPUTERISED CIRCUIT ANALYSIS

Designing amplifier circuits? This article shows how to design programs to take the sweat and guesswork out of the operation.

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MOST READERS of this magazine will, sooner or later, find themselves in a position where they have to design basic amplifier circuits. This need not be a tedious and time-consuming task if you develop some of the ideas presented in this article. We have included a demonstration program for the sake of interest, but the object of this exercise is to show you how to go about the problem of designing with a computer. You can write your own program to suit your own computer and your own design.

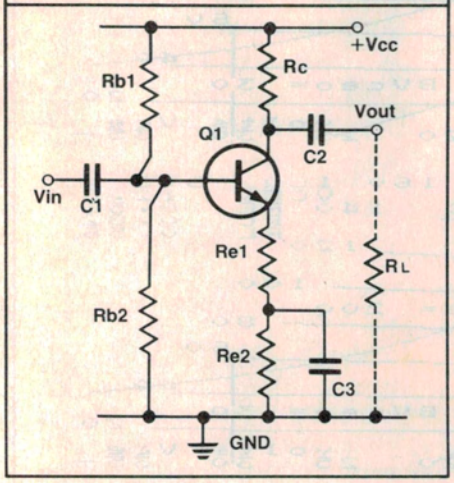
The fundamental circuit for a Class A amplifier is given in Figure 1. The first step in analysing a transistor circuit is to establish the biasing, since it is this that sets up the effective gain of the amplifier. For the circuit in Figure 1 the first step is to establish the base voltage, Vb. A standard but simplified equation which allows a quick solution is:

$$Vb = \frac{Rb2 \times Vcc}{Rb1 + Rb2}$$

From this we can determine Ve very quickly if we assume that there will be a drop of about 0.6 V across the base-emitter junction of the transistor:

$$Ve = Vb - 0.6$$

Figure 1. General form of the Class A voltage amp.



We now have access to the current flowing in the emitter resistor from Ohm's law, since we know the voltage across the resistor and its value:

$$Ie = \frac{Ve}{Re}$$

where Re = Re1+Re2.

Since we also know that the emitter current must be more or less the same as the collector current we can also work out the collector voltage:

$$Vc = Vcc - RcIc$$

AC response

With this series of simple steps we have worked out all the voltages around the transistor plus the current flowing between the collector and the emitter. We are now in a position to begin an examination of the circuit's response to an input signal, i.e: its ac response.

The gain of an amplifier is given by:

$$Av = \frac{\text{collector load}}{\text{emitter load}}$$

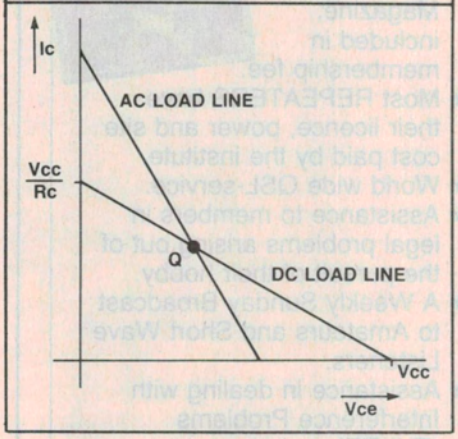
Bear in mind that these values apply to ac conditions only. The collector load includes all the resistances that tie the collector to either the ground or supply rails. (Supply is ac-shorted to ground through the power supply.) It includes at least the collector resistor Rc, the load resistance R1 and the collector-emitter leakage resistance. This latter is usually so high that it can be ignored in low frequency, small signal applications.

The emitter load, likewise, includes all the resistances between the emitter of the transistor and either rail. In practice this will mean the unbypassed emitter resistor Re1, but not Re2. Remember we are talking about ac and assuming that all the capacitors are short circuits, so Re2 is effectively shorted. It also includes the base-emitter resistance, r_e, which is given by 30/Ic.

The result of this is that we can establish a gain equation for the circuit of Figure 1:

$$Av = \frac{Rc}{r_e + Re1}$$

Figure 2. Plotting the ac and dc load lines.



Obviously, different configurations will have different equations, but the principle remains the same, so you can work out the relevant equation for your particular application.

So far, we have sufficient information to generate a program that will predict certain elements of the performance of an amplifier given the circuit. If you input the values of the resistors the program should come back at you with the gain. If you go to a textbook you should be able to extract equations to give you input and output resistance as well.

The question not answered, and the one we would like to know, is whether the combination of resistors we have chosen is an optimum. The classic method of doing this is with the *load line*.

Load Lines

Load line analysis involves drawing a pair of straight lines corresponding to the ac and dc loads on the transistor. It is actually a graph of Ic and against Vce. The load line is thus all the possible combinations of Ic and Vce that can exist at the collector of the particular amplifier under consideration.

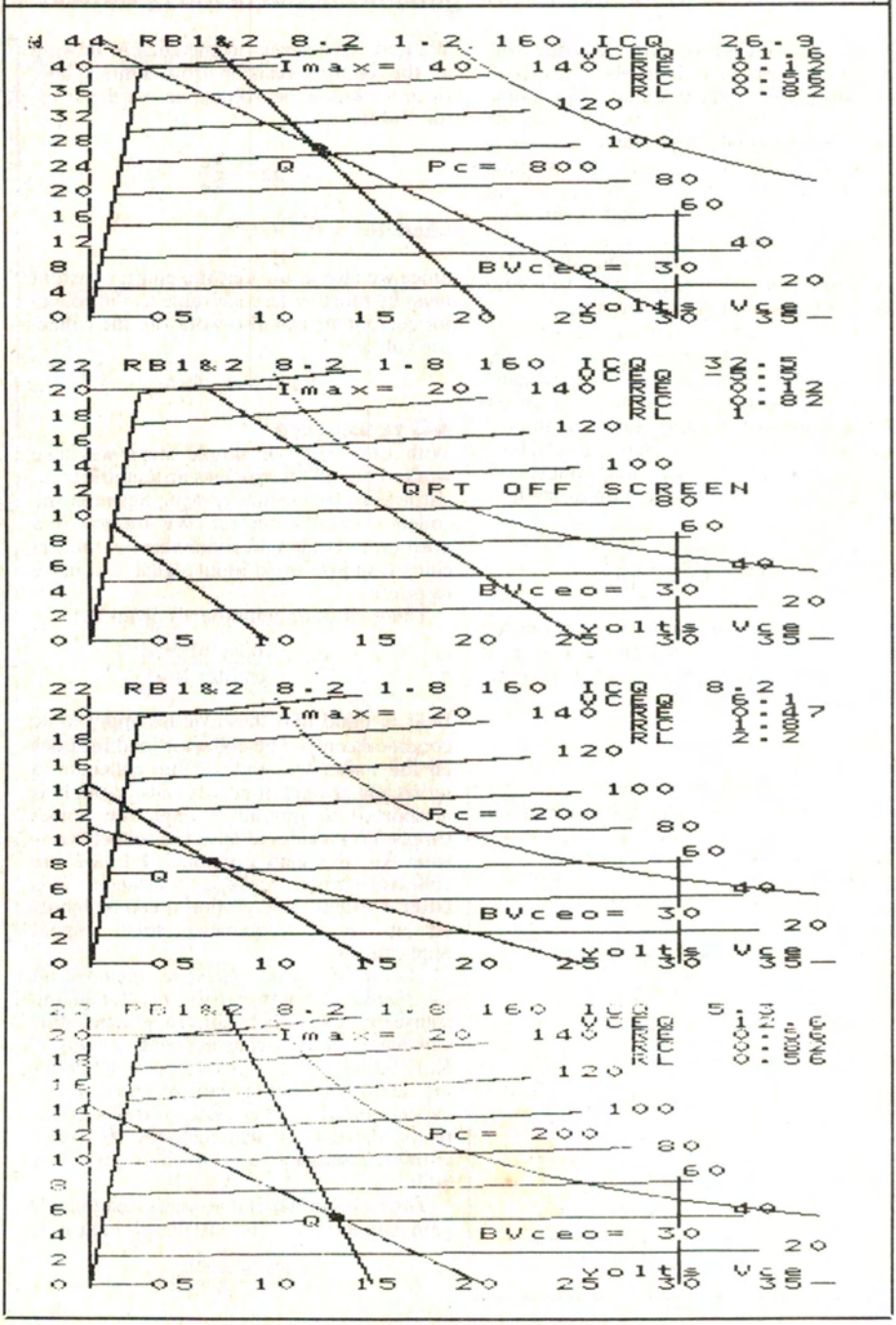
We can determine the dc line quite easily (see Figure 2). When no current flows i.e: Ic=0, then Vce=Vcc. This defines the bottom point of the line; i.e: the intersection with the horizontal axis. At the other end of the line, when Vce is at a minimum, Ic is ▶

determined by the value of the resistors through which it flows (Vce is assumed to be zero). The dc load line is just a straight line between these two points.

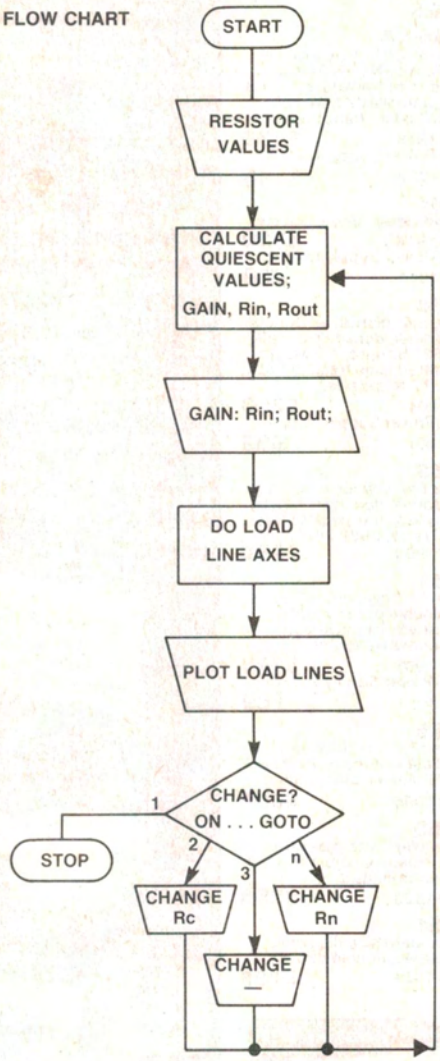
The operating point, Q, at which the amplifier is biased, must lie somewhere on this line. The ac line intersects the dc line at this point. It is drawn with slope equal to the inverse of the ac collector load. For an unloaded amplifier this will just be Rx, with the result that the ac slope will be the same as the dc slope. However, when the amplifier is loaded the slope of the line will tend to increase as the total collector resistance decreases.

As with the dc load line, the ac line determines the combination of values of Ic and Vce that can exist in the amplifier with a ▶

The plot quickens. Screen dumps of load lines plotted by the program over the page. The beauty of the technique is its ability to show the results of any variation quite quickly.



FLOW CHART



specific load. We are now in a position to ask the question about the amplifier we have designed, namely: what is the maximum output voltage I can get from this amplifier without distortion? In most applications the aim of the exercise, after all, is to magnify the input as much as possible while distorting it as little as possible.

Non-linearities

Non-linearities will occur whenever the output gets close to either end of the load line. Clipping will occur if you try to push the output past it. The idea then is to arrange your gain for a given input such that it can drive the output close to, and not right to, the end of the line. You also want to arrange things such that both positive and negative voltage excursions begin to slip at the same time. There is no point building something that will leave the positive side of the wave unclipped while distorting the negative wave badly. This state of affairs will come about when the Q point, i.e: the quiescent voltage of the transistor collector

PROGRAM LISTING

```
10 REM*********************************
11 REM* THIS PROGRAM PLOTS A SET OF   *
12 REM*TRANSISTOR CHARACTERISTICS WHEN*
13 REM*CERTAIN PARAMETERS ARE ENTERED.*
14 REM*THEN LOAD LINES ARE PLOTTED FOR*
15 REM*VARIOUS VALUES OF COMPONENTS.  *
16 REM*********************************
35 PAPER 1: INK 7
38 PRINT "*****************************"
39 PRINT "*                           *"
40 PRINT "* *  *   *  **  *  * * * ***"
41 PRINT "* * * * * * * *  * *** * **"
42 PRINT "* * * * *** * * *  * *** ***"
43 PRINT "* * * * * * * * *  * *** * *"
44 PRINT "* ** *  * * **  ** * * * ***"
45 PRINT "*                           *"
46 PRINT "*    LANCE WILSON, 1984     *"
47 PRINT "*                           *"
48 PRINT "*****************************"
49 PAUSE 2000
50 CLS
55 REM**WRITTEN FOR THE MEMOTECH*****
56 REM**         MTX500          *****
57 REM**GRAPHICS DUMP FOR CP80 PRINTER*
58 REM~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
65 REM*THESE LINES SET VIRTUAL SCREENS,
66 REM*1ST FOR TEXT, THEN GRAPHICS.
70 CRVS 2,0,3,0,36,5,40
75 VS 2: CLS : PAPER 6: INK 7
80 CSR 4,0: INPUT "COMPLEX:Y/N?";A$
81 LET PMAX=200
82 LET VSF=2: LET ICMAX=20
83 LET BVCEO=30: LET HFE=100
84 IF A$="N" THEN  GOTO 100
85 CLS : CSR 4,0: INPUT "HFE:?";HFE
86 CSR 4,1: INPUT "MAX PC:?";PMAX
88 CSR 4,2: INPUT "ICmax:?mA";ICMAX
90 CSR 4,3: INPUT "BVCEO:?";BVCEO
92 LET VSF=INT(ICMAX/10)
100 CLS
102 CSR 4,0: INPUT "    ENTER STEP";STP
104 CLS : CSR 4,0: INPUT " ENTER Vcc";VCC
105 CSR 4,0: INPUT " EMITTER&COLLECTOR R";RE,RC
106 CSR 4,3: INPUT "RB1,RB2= ?";RB1,RB2
107 LET ID=VCC/(RB1+RB2)
108 VS 4: CLS : COLOUR 2,11: COLOUR 3,4
109 COLOUR 0,1: COLOUR 1,15: COLOUR 4,6
110 REM**SETS UP AXES AND SCALES*******
111 LINE 20,12,255,12: LINE 20,12,20,190
112 CSR 5,22: PRINT "05  10  15  20  25  30  35"
113 CSR 22,21: PRINT "volts Vce"
114 FOR I=0 TO 11 STEP 1
115 CSR 0,(11-I)*2: PRINT I*VSF
117 NEXT I
118 REM**DRAWS CHAR. CURVES      *******
119 LET X=20: LET Y=10
120 LET NEWX=X+STP/10: LET NEWY=Y+STP
122 LINE X,Y,NEWX,NEWY
123 LINE NEWX,NEWY,250-.8*Y,NEWY*1.11
125 CSR 30-Y/12,21-Y/7: PRINT Y+10
126 LET X=NEWX: LET Y=NEWY
127 IF Y>150 THEN  GOTO 130
128 GOTO 120
129 REM*AFTER TOP CURVE, PLOT PCMAX
130 FOR I=1 TO 230
135 LET YP=PMAX*100/(VSF*I)
140 IF YP>175 THEN  GOTO 150
142 COLOUR 3,6
145 PLOT 20+I,YP+12
150 NEXT I
151 CSR 16,10: PRINT "Pc=";PMAX
153 REM******UPPER IC & VCE LIMITS*****
154 LET ILIM=ICMAX*16/VSF+12: IF ILIM>190 THEN  GOTO 990
155 LINE 20,ILIM,80,ILIM
156 CSR 10,22-ILIM/9: PRINT "Imax=";ICMAX
157 LET VLIM=BVCEO*6.2+20: IF VLIM>250 THEN  GOTO 990
158 LINE VLIM,12,VLIM,80: CSR VLIM/9-4,18: PRINT "BVceo=";BVCEO
159 REM****NEXT CALCS. FOR QPT. AND****
160 REM****** DC LOAD LINE ************
161 LET ICQ=((RB2*VCC)/(RB1+RB2)-.6)/RE
```

```
162 LET IBQ=ICQ/HFE
163 IF IBQ*6>ID THEN  GOTO 300
165 LET VCEQ=VCC-ICQ*(RC+RE)
170 LET IQX=ICQ*16/VSF+12
175 LET VQX=VCEQ*6.2+20
177 IF VQX>250 OR IQX>190 THEN  GOTO 850
179 IF VCEQ<0 THEN  GOTO 2000
180 CIRCLE VQX,IQX,2
185 CSR .8*VCEQ+1,22-1.65*ICQ/VSF: PRINT "Q"
190 CSR 22,0: PRINT "ICQ ";INT(ICQ*10)/10
191 CSR 22,1: PRINT "VCEQ ";INT(10*VCEQ)/10
192 CSR 24,2: PRINT "RE ";RE
193 CSR 24,3: PRINT "RC ";RC
194 CSR 4,0: PRINT "RB1&2";RB1;RB2
199 GOTO 800
300 REM**
305 VS 2: CLS
308 LET S=ID/IBQ
310 CSR 6,10: PRINT "Id/Ib Ratio is ";S
311 CSR 8,12: PRINT ":rather low!"
315 PAUSE 8888
320 GOTO 106
400 REM****** AC LOAD LINE ***********
405 VS 2: CLS
410 INPUT "RE BYPASSED?";A$
420 INPUT "RL=? ";RL
425 LET RAC=(RC*RL)/(RC+RL)
430 LET VPK=ICQ*RAC
435 LET VPX=(VCEQ+VPK)*6.2+20
440 VS 4
443 CSR 24,4: PRINT "RL ";RL
445 LINE VPX,12,VQX,IQX
450 LET IPK=ICQ+VCEQ/VPK*ICQ
455 LET IPX=IPK*16/VSF+12
457 IF IPX>192 THEN  GOTO 480
460 LINE VQX,IQX,20,IPX
470 PAUSE 7777
475 GOTO 1000
479 REM***** LIMIT CONDITIONS *********
480 LET IPX=190: LET IPK=(IPX-12)*VSF/16
482 LET VA=VCEQ-RAC*(IPK-ICQ)
483 LET VAX=VA*6.2+20
484 LINE VQX,IQX,VAX,IPX
488 PAUSE 7777
489 GOTO 1000
800 REM
810 LET IX=VCC/(RE+RC)*16/VSF+12
812 LET VX=VCC*6.2+20: REM SCALEUNITS
814 IF IX>190 THEN  GOTO 900
815 LINE 20,IX,VX,12
820 PAUSE 8888
830 GOTO 400
850 REM*********************************
855 CSR 15,10: PRINT "QPT OFF SCREEN"
860 GOTO 190
900 REM*TO COVER OFF-SCALE LOADLINE
905 LET IC=ICMAX
906 LET IX=IC*16/VSF+12
910 LET VX=(VCC-IC*(RC+RE))*6.2+20
916 PAUSE 9000
920 LINE VCC*6.2+20,12,VX,IX
930 GOTO 830
990 CSR 5,2: PRINT "ICMAX OFF SCREEN"
998 STOP
999 REM**********GRAPHICS DUMP**********
1000 LPRINT CHR$(27);"A";CHR$(8);
1010 FOR J=191 TO 0 STEP -8
1020 LPRINT CHR$(13);CHR$(10);
1030 LPRINT CHR$(27);"K";CHR$(254);CHR$(1);
1040 FOR I=1 TO 255
1050 LET R$=GR$(I,J,8)
1060 LPRINT R$;: LPRINT R$;
1070 NEXT I
1080 NEXT J
1099 STOP : REM************************
2000 VS 2: CLS
2001 PRINT "NEGATIVE COLLECTOR VOLTAGE"
2002 PRINT "NOT ALLOWED"
2004 PAUSE 7777
2005 GOTO 104
```

is midway between the maximum voltage excursions.

Departures

To get this far in the analysis we have made certain assumptions about the circuit which are not strictly true. Whether they are significant or not depends on the individual case. It is important to realise they are there, however, so that if you start getting results that are not as predicted you know where to look.

The first problem is that the transistor has a saturation voltage that depends primarily on the current. Saturation voltage is drawn on a load line diagram as part of the transistor collector characteristics. Usually these are drawn as a family of curves indicating the relationship between collector current and voltage for a given base current. These curves will be more or less flat in the linear operating region of the transistor, falling off on the left-hand side as the transistor goes into saturation.

In order to achieve a really accurate determination of the transistor characteristic you ideally need to make a plot for each individual transistor. Failing that, manufacturers' data is a good source for typical figures. However, for our purposes it is probably just as useful if you think of the transistor characteristic as a line passing through the origin. The slope is set by at least one typical combination of current and voltage supplied from manufacturer's data. If you don't have access to this information then a value of 0.3 V at 2 mA is typical for small signal transistors.

A second source of errors is likely to be the assumption that all the capacitors are short circuits and that stray capacitances around the circuit are negligible. As frequency goes up this will become more and more of a problem.

So far, we have thought through this problem as a simple linear process, a not very difficult programming exercise involving a few calculations and the ability to draw some lines. This doesn't really explore the potential of the computer in this regard, though. Its biggest advantage is the fact that you can very quickly see what happens to a host of different parameters of the amplifier if you change values of any of the biasing resistors, or indeed if you change resistor configurations.

We have included a flow chart that should give you some idea of how to go about writing the program. It includes a menu for making individual changes to resistors and then re-running to see the effect. We have also included a listing of a BASIC program that draws a load line diagram complete with transistor characteristics and both load lines. This is written for the Memotech computer and so will need to be rewritten by anyone using a different type of machine, but close study of how it works will be instructive.

Good luck! ●